IN THE CLAIMS

What is claimed is:

1. A semiconductor integrated circuit device, comprising:

a plurality of insulated gate field effect transistors (IGFETs) coupled to a corresponding input/output (I/O) terminal through a corresponding first resistance;

a first clamping device coupled to each I/O terminal;

a second clamping circuit corresponding to each IGFET, each second clamping circuit including a second clamping device and the corresponding first resistance, each second clamping device having a first terminal connected to a gate electrode of the corresponding IGFET and a second terminal connected to a source/drain terminal of the corresponding IGFET and a supply potential wiring;

each first clamping device being coupled to one second clamping device through a second resistance; and

at least two of the second clamping circuits vary from one another.

2. The semiconductor integrated circuit device method of claim 1, wherein:

a supply potential wiring is selected from the group consisting of an electric power supply potential wiring, a ground electric potential wiring, and a substrate electric potential wiring.

3. The semiconductor integrated circuit device of claim 1, wherein: the at least two second clamping circuits vary by the second clamping device of one second clamping circuit having a different capability than the second clamping device of the other second clamping circuit.

4. The semiconductor integrated circuit device of claim 1, wherein: the at least two second clamping circuits vary by a first resistance (Rin) of one second clamping circuit having a different value than the first resistance (Rin) of the other second clamping circuit, and a ratio between the second resistance and the first resistance (Rg/Rin) for both clamping circuits having a predetermined maximum value.

5. The semiconductor integrated circuit device of claim 1, wherein: a length of a wiring that connects the second clamping devices to the gate electrode of the corresponding IGFETs is no more than 100 micrometers.

6. The semiconductor integrated circuit device of claim 1, wherein: a length of a wiring that connects the second clamping devices to the source/drain electrode of the corresponding IGFETs is no more than 100 micrometers.

7. The semiconductor integrated circuit device of claim 1, wherein: the first resistance comprises essentially a wiring resistance and a

contact resistance.

8. The semiconductor integrated circuit device of claim 1, wherein:

the majority of at least one first resistance includes non-wiring structures.

9. The semiconductor integrated circuit device of claim 1, wherein:

at least one first resistance includes an effective channel resistance of an input path IGFET.

10. The semiconductor integrated circuit device of claim 1, wherein:

the second resistance comprises essentially a supply potential wiring resistance and a contact resistance where the first and second clamping devices are connected to the supply potential wiring.

11. The semiconductor integrated circuit device of claim 1, wherein:

each first clamping devices has a first terminal connected to one of the I/O terminals and a second terminal, the second terminals of each first clamping device being connected to the second terminal of one of the second clamping devices by system wiring of at least one supply terminal; and

the second resistance comprises essentially a contact resistance between the second terminal of the first clamping device and the supply potential wiring, a supply potential wiring between the first clamping device

and the supply terminal, a supply terminal resistance, a supply potential wiring between the supply terminal and the second terminal of the second clamping device, and a contact resistance between the second terminal of the second clamping device and the supply potential wiring.

12. The semiconductor integrated circuit device of claim 1, wherein:

each first clamping device has a first terminal connected to one of the I/O terminals and a second terminal connected to a first supply terminal; and

the second terminal of each second clamping device is connected to a second supply terminal different from the first supply terminal.

13. The semiconductor integrated circuit device of claim 12, wherein:

the first and second supply terminals are connected to one another through a conductive integrated circuit package structure.

14. The semiconductor integrated circuit device of claim 1, wherein:

at least a portion of each second clamping device is selected from the group consisting of an IGFET having a source/drain coupled to a gate, an NPN bipolar device, a diode, and a thyristor.

15. The semiconductor integrated circuit device of claim 1, wherein:

the at least two second clamping circuits vary by the second clamping device of one second clamping circuit having a different construction than the

second clamping device of the other second clamping circuit.

16. A method for designing a protective circuit for a semiconductor integrated circuit device that includes insulated gate field effect transistors (IGFETs) formed thereon, the method comprising the steps of:

executing a simulation with a predetermined charged device model (CDM) equivalent circuit that includes a first clamping device connected to an input/output (I/O) terminal, a first IGFET having a gate connected to the I/O terminal through a first resistance (Rin), a second clamping device connected between gate and source/drain terminals of the first IGFET and connected to a supply potential wiring, the first and second clamping devices being connected to one another through a second resistance (Rg); and

selecting a ratio of the second resistance and the first resistance (Rg/Rin) that prevents a potential between the gate and source/drain terminal of the first IGFET from exceeding a predetermined value.

17. The method of claim 16, wherein:

the predetermined value is determined from a relationship between CDM test results and ratios of the second resistance and the first resistance (Rg/Rin), and simulation results showing a relationship between a potential between the gate and source/drain terminal of the first IGFET and ratios of the second resistance and the first resistance (Rg/Rin).

18. The method of claim 16, wherein:

the first and second resistance values are set to ranges that ensure predetermined circuit characteristics.

19. The method of claim 16, further including:

changing the properties a second clamping device for a second IGFET to prevent a potential between the gate and source/drain terminal of the first IGFET from exceeding a predetermined value.

20. The method of claim 19, wherein:

the changing the properties of the second clamping device includes changing the size of the second clamping device.